REMARKS

Claims 13, 31-35, and 53 are amended, and claims 54-62 are added. Claims 13, 21-26, and 28-62 are pending, where claims 13, 21, 31, 34, 35, 41, and 50 are independent claims. The Applicant has carefully and thoughtfully considered the Office Action mailed February 6, 2004 and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

1. In the Office Action on page 2 in section 1, claim 49 is objected to as not including all the limitations of claim 41. Claim 49 is a dependent claim and depends from claim 41. By definition, claim 49, as being dependent from claim 41, includes all the limitations of claim 41. See 37 C.F.R. § 1.75(c) ("One or more claims may be presented in dependent form, referring back to and further limiting another claim or claims in the same application... Claims in dependent form shall be construed to include all the limitations of the claim incorporated by reference into the dependent claim."). Hence, the objection is respectfully requested to be rescinded.

2. On page 2, claims 13, 21-26, 28-33, and 35-53 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,575,844 to Kosuge et al. (hereinafter Kosuge). The Applicant respectfully traverses the rejections.

Claim 13

Claim 13 recites a switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports. The switch comprises: means for switching a TDM data

from an input port to an output port, comprising means for storing the TDM data in a single shared memory based on a time slot of a frame in which the TDM data was received; and means for switching a packet data from an input port to an output port, comprising means for storing the packet data in said single shared memory based on routing data embedded in the packet data and based on the input port which received the packet data.

Kosuge teaches a digital switching system in Figure 1 having a hierarchical storage. Referring to Figure 1, the hierarchical storage 10 includes a small-capacity high-speed memory 11, a large-capacity low-speed memory 12, and a file memory 13. Kosuge, column 3, lines 24-39. Referring to Figures 3, 6 and 11, a circuit switching call address generator 403 (of Figure 6, and expanded in Figure 11) in step 106 (of Figure 3) selects a cache address CAD for storing data for a circuit switching call in the circuit switching call buffer of the memory 11. Kosuge, column 4, lines 64-67; column 6, lines 38-42; column 9, lines 48-64. Referring to Figure 13, addresses for storing data for a circuit switching call in the circuit switching call buffer of the memory 11 are selected based on "do not block replacement prevention" flags 21 and "block replacement order" flags 22. Kosuge, column 11, line 49, to column 12, line 29. Referring to Figures 3, 6, and 12, a packet switching call address generator 404 (of Figure 6, and expanded in Figure 12) in step 404 (of Figure 6) selects a virtual address for storing data for a packet switching call, a memory management block 405 (of Figure 6) in step 108 (of Figure 3) converts the virtual address to a real address, and a cache access management block 406 (of Figure 6) in step 109 (of Figure 3) converts the real address to a cache address CAD for storing data for the packet switching call in the packet switching call buffers of the memories 11, 12, and 13. Kosuge, column 4, line 67, to column 5, line 5; column 6, lines 42-46; column 9, line 65, to column 11, line 48. Kosuge, however, fails to teach at least **three** aspects of claim 21.

First, Kosuge fails to teach storing the TDM data in a single shared memory based on **a time slot of a frame** in which the TDM data was received. As generally noted by the Office Action, Kosuge teaches in Figures 3, 6, 7, and 11, that a memory management block 401 (of Figure 6, and expanded in Figure 7) in steps 100-102 (of Figure 3) provides signals INL and INLAD in steps 111-113 (of Figure 7) to a circuit switching call address generator 403 (of Figure 6). Kosuge, column 6, lines 34-36; column 7, lines 10-12, 34-45. Thereafter, the circuit switching call address generator 403 (of Figure 6, and expanded in Figure 11) in step 106 (of Figure 3) selects a cache address CAD for storing data for a circuit switching call in the circuit switching call buffer of the memory 11. Kosuge, column 4, lines 64-67; column 6, lines 34-36, 38-42; column 7, lines 10-12, 42-45; column 9, lines 48-64. Kosuge, however, **fails** to store the data for a circuit switching call based on **a time slot of a frame** in which the data for a circuit switching call was received.

Instead, Kosuge teaches in Figure 13 storing the data for a circuit switching call in memory 11 based on **"do not block replacement prevention" flags 21** and **"block replacement order" flags 22**. Kosuge, column 11, lines 49-58. The "do not block replacement prevention" flags 21 and "block replacement order" flags 22 are **unrelated** to a time slot of a frame in which the data for a circuit switching call was received. In particular, Kosuge teaches that the block of memory 11 having the largest value for the "block replacement order" flag 22 is subject to replacement, unless the value for the "do not block replacement prevention" flag 22 is set to "1". Kosuge, column 12, lines 10-29. In Figure 13, memory 11 includes data R0 to R4 for circuit switching calls in block 0 for columns 0 to 7 and in block 1 for columns 0 to 1 but includes no data for any circuit switching call in block 1 for columns 2 to 7. Kosuge, column 12, lines 10-11. As an example on how the flags 21 and 22 are used to store data in the memory 11,

for block 0 in column 1, memory 11 holds data "R0", flag 22 is set to "4", and flag 21 is set to "1", and the maximum value discriminator 23 outputs a "4". Hence, block 0 in column 1 of memory 11 is not subject to replacement. Kosuge, column 11, lines 59-67. Thus, according to Kosuge, the data for circuit call switching are **not** stored in the memory 11 based on **a time slot of a frame** in which the data for a circuit switching call was received but are, instead, stored in the memory 11 based on **"do not block replacement prevention" flags 21** and **"block replacement order" flags 22**. Hence, claim 13 is allowable for a first reason.

Second, Kosuge fails to teach storing packet data in a single shared memory based on **routing data embedded in the packet data** and based on the **input port which received the packet data**. As generally noted by the Office Action, Kosuge teaches in Figures 3, 6, 7, and 12, that a memory management block 401 (of Figure 6, and expanded in Figure 7) in steps 100-102 (of Figure 3) provides signals INL and INLAID in steps 121-126 (of Figure 7) to a packet switching call address generator 404 (of Figure 6). Kosuge, column 6, lines 34-36; column 7, lines 10-12; column 7, line 46, to column 8, line 4. Thereafter, the packet switching call address generator 404 (of Figure 6, and expanded in Figure 12) in step 404 (of Figure 6) selects a virtual address for storing data for a packet switching call, a memory management block 405 (of Figure 6) in step 108 (of Figure 3) converts the virtual address to a real address, and a cache access management block 406 (of Figure 6) in step 109 (of Figure 3) converts the real address to a cache address CAD for storing data for the packet switching call in the packet switching call buffers of the memories 11, 12, and 13. Kosuge, column 4, line 67, to column 5, line 5; column 6, lines 42-46; column 9, line 65, to column 11, line 48. Kosuge, however, **fails** to store the data for a packet switching call based on **routing data embedded in the packet data** and based on the **input port which received the packet data**.

Instead, using the same technique discussed above for storing the data for a circuit switching call, Kosuge teaches in Figure 13 storing the data for a packet switching call in memories 11, 12, and 13 based on **"do not block replacement prevention" flags 21** and **"block replacement order" flags 22**. Kosuge, column 11, lines 49-58. The "do not block replacement prevention" flags 21 and "block replacement order" flags 22 are **unrelated** to the routing data embedded in the packet data and based on the input port which received the packet data. In particular, Kosuge teaches that the block of memory 11 having the largest value for the "block replacement order" flag 22 is subject to replacement, unless the value for the "do not block replacement prevention" flag 22 is set to "1". Kosuge, column 12, lines 10-29. As illustrated in Figure 13, memories 11 and 12 include data A and C for packet switching calls in various columns of blocks 2 and 3. Kosuge, column 12, lines 11-13. As an example on how the flags 21 and 22 are used to store data in the memories 11 and 12, when a block within a portion "Y" in memory 12 is to be transferred, the data A in column 1 of block 2 in the memory 11 is replaced per the flags 21 and 22. Kosuge, column 11, line 59, to column 12, line 29. Thus, according to Kosuge, the data for packet call switching are **not** stored in the memories 11, 12, and 13 based on **routing data embedded in data for a packet switching call** and based on the **input port which received the data for a packet switching call** but are, instead, stored in the memories 11, 12, and 13 based on **"do not block replacement prevention" flags 21** and **"block replacement order" flags 22**. Hence, Kosuge fails to teach the claimed invention.

In addition, in rejecting claim 13, the Office Action also relies on the recitations of claims 2 and 3 in columns 13-14 of Kosuge. These two claims, however, **fail** to teach, or even fairly suggest, storing a packet data in a single shared memory based on **routing data embedded in the packet data** and based on the **input port which received the packet data**. Instead, claim 2

of Kosuge claims that the hierarchical storage (item 10 in Figures 1 and 6 of Kosuge) comprises a file memory (item 13 in Figures 1 and 6 of Kosuge) for storing packet switching data corresponding to packet switching calls. Further, claim 3 of Kosuge claims that the hierarchical storage (item 10 in Figures 1 and 6 of Kosuge) is commonly used for a switching program together with the circuit and packet switching calls. **Neither** claim 2 **nor** claim 3 have any teachings related to storing a packet data in a single shared memory based on routing data embedded in the packet data and based on the input port which received the packet data. Hence, claim 13 is allowable for a second reason.

Third, Kosuge fails to teach a **single shared memory** for storing both TDM data and packet data. In rejecting claim 13, the Office Action aligns the recited single shared memory with the memory 11, memory 12, and memory 13 in Figure 1 of Kosuge. The Office Action lumps these **three separate memories** together and asserts that the hierarchical storage 10 in Figure 1 of Kosuge is the same as the recited **single shared memory**. The hierarchical storage 10 of Kosuge, however, consists of three separate and distinct memories, namely the small-capacity high-speed memory 11, the large-capacity low-speed memory 12, and the file memory 13. Kosuge, Figure 1; column 3, lines 24-27; column 6, lines 8-25. For circuit switching, the small-capacity high-speed memory 11 is used. Kosuge, column 1, lines 64-66; column 3, lines 29-35; column 6, lines 4-8 and 15-18; Figures 4 and 5. For packet switching, the small-capacity high-speed memory 11, the large-capacity low-speed memory 12, and the file memory 13 are used. Kosuge, column 1, lines 64-66; column 3, lines 29-39; column 6, lines 8-14 and 18-25; Figures 4 and 5.

Contrary to the understanding by the Examiner, the claim, however, does not recite **multiple** shared memories, but instead recites a **single** shared memory. By using **multiple**

shared memories, instead of a **single** shared memory, the system of Kosuge requires additional hardware and software than is required when using the claimed invention. The following Table A summarizes the additional hardware and software needed by Kosuge to use multiple shared memories.

Table A
Kosuge's hardware and software needed to implement multiple shared memories

Storing circuit switching data in Kosuge	**Storing packet switching data in Kosuge**	***Additional* hardware and software needed in Kosuge to implement multiple shared memories**
single memory 11 (in Figures 1 and 6)	three memories 11, 12, and 13 (in Figures 1 and 6)	*memories 12 and 13 (in Figures 1 and 6)*
circuit switching call address generator 403 (in Figure 6, expanded in Figure 11)	packet switching call address generator 404, memory management block 405, and cache address management block 406 (in Figure 6, expanded in Figure 12)	*memory management block 405, and cache address management block 406 (in Figure 6), and increment and counter of register array 4040, adder 4041, steps 4043 and 4044 (compare Figures 11 and 12)*
step 106 (in Figure 3)	steps 107, 108, 109, and 110 (in Figure 3)	*steps 108, 109, and 110 (compare flow for circuit switching call and packet switching call in Figure 3)*
steps 111, 112 and 113 (in Figure 7)	steps 121, 122, 123, 124, 125, and 126 (in Figure 7)	*steps 121, 122, 123, and 124 (compare flow for circuit switching call and packet switching call in Figure 7)*
a cache address CAD	a virtual address, a real address, and a cache address CAD	*virtual address and real address*

For circuit switching, see Kosuge, column 4, lines 64-67; column 6, lines 34-36, 38-42; column 7, lines 10-12, 34-45; column 9, lines 48-64. For packet switching, see Kosuge, column 4, line 67, to column 5, line 5; column 6, lines 34-36, 42-46; column 7, lines 10-12; column 7, line 46, to column 8, line 4; column 9, line 65, to column 11, line 48. Because Kosuge uses multiple shared memories, more hardware and software is required than if a single shared memory was used. Hence, Kosuge fails to both anticipate and render obvious this feature of the claimed invention. Thus, claim 13 is allowable for a third reason.

Claims 21-30

Claim 21 recites a switch to switch TDM data and packet data from input ports to output ports. The switch comprises: a plurality of input ports to receive data, wherein each data comprises either TDM data or packet data; a plurality of output ports to transmit switched data; a single shared memory coupling the input ports to the output ports; a time slot interchange controller coupled to the single shared memory to select addresses in the single shared memory to store TDM data; and a packet switch controller coupled to the single shared memory to select addresses in the single shared memory to store packet data. The single shared memory is adapted to receive sequentially all TDM data and all packet data received from the input ports, store both TDM data and packet data, and switch all sequentially received TDM data and packet data received from respective input ports to respective output ports. Switching of any received TDM data is based on input time slots of the TDM data. The time slot interchange controller is adapted to select an address of the single shared memory for a TDM data based on a time slot of a frame in which the switch received the TDM data. The packet switch controller is adapted to select an address of the single shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data.

For at least four reasons, Kosuge fails to teach claim 21. First, Kosuge fails to teach a time slot interchange controller to select an address of a single shared memory for a TDM data based on a time slot of a frame in which the TDM data was received. Based on the same analysis presented above for the first reason regarding claim 13, claim 21 is allowable for a first reason.

Second, Kosuge fails to teach a packet switch controller to select an address of a single shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data. Based on the same analysis presented above for the second reason regarding claim 13, claim 21 is allowable for a second reason.

Third, Kosuge fails to teach a single shared memory. Based on the same analysis presented above for the third reason regarding claim 13, claim 21 is allowable for a third reason.

Fourth, Kosuge fails to inherently teach a time slot interchange controller. In rejecting claim 21, the Office Action correctly asserts that Kosuge fails to teach the recited time slot interchange controller, but incorrectly asserts that the recited time slot interchange controller is inherently taught by Kosuge. Contrary to this ***inherency*** assertion by the Office Action, Kosuge teaches in Figure 1 switching of circuit data based on **control data extracted** from a **common control channel signal** received by a signal reception circuit 17 from the TDM transmission input lines 15. Kosuge, column 3, line 66, to column 4, line 4. Under control of the processor 18 in Figure 1 of Kosuge, the control section 14 switches TDM data based on the control data extracted from the common control channel signal. Kosuge, column 4, lines 4-6. As illustrated in Figure 2 of Kosuge, the control data extracted from the common control channel signal includes **five data types**: a service indicator A indicating circuit switching or packet switching; a terminal indicator B indicating the terminal type for circuit switching or packet switching; a signal indicator C including supervisory signals, such as an originating signal, a disconnect signal, and an off-hook signal; a rate indicator D including transmission rate data; and a selection data E including a dialing signal. Kosuge, column 4, lines 7-23. **None** of these five data types of Kosuge correspond to selecting an address of a single shared memory for a TDM data based on a **time slot** of a **frame** in which the TDM data was received. Hence, Kosuge fails to teach,

inherently teach, or fairly suggest, the recited time slot interchange controller, and claim 13 is allowable for a fourth reason.

Claims 22-26 and 28-30 are dependent from claim 21 and are allowable as being dependent from an allowable claim.

Further, claim 24 recites that the single shared memory is adapted to treat the input ports as **logical input ports**. In rejecting claim 24, the Office Action aligns the recited logical input ports with the terminals in Figure 1 of Kosuge. However, in rejecting claim 21, the Office Action also aligns the recited input ports with the terminals in Figure 1 of Kosuge. As discussed in the specification, logical input ports are, for example, are groupings of time slots in frames received at the input ports to obtain a channel capacity greater than that provided by a single time slot. See, e.g., specification, page 7, lines 19-21. In contrast, Kosuge discusses in Figure 3 and 4 **multiplexing time slots** from the input line attached to the terminals in Figure 1 due to the serial processing nature of the system, but does **not** discuss treating the input ports as logical input ports. Kosuge, column 2, lines 33-39; column 3, lines 56-60; column 3, line 66, to column 4, line 4; column 4, lines 44-48; column 5, lines 56-62. Hence, claim 24 is allowable.

Claim 25 recites that the single shared memory is adapted to place **sequentially** received packet data in **a queue for a respective output port**. In rejecting claim 25, the Office Action aligns the recited queue for a respective output port as data being received at the switch memory to transmit to the output. The Office Action fails to point to any citation in Kosuge in rejecting claim 25. In Figure 5, Kosuge teaches how packet switching data is switched from inputs to outputs. Kosuge, column 6, lines 1-32. In Figure 13, Kosuge teaches how packet switching data is stored in the three memories 11, 12, and 13. Kosuge, column 11, line 49, to column 12, line 29. However, in discussing how data is switched and stored, Kosuge fails to mention that

sequentially received packet data is placed in a **queue** for a **respective output port**. Hence, claim 25 is allowable.

Claim 26 recites that the data are **received** by the input ports and **transmitted** by the output ports as **data exchange units**. In rejecting claim 26, the Office Action aligns the recited data exchange units with **TDM** with time frames as exchange units to transmit data **from** input **to** output port. The Office Action fails to point to any citation in Kosuge in rejecting claim 26. As discussed in the specification, data exchange units are, for example, used to transfer data between a switch and an I/O channel card. See, e.g., specification, page 12, lines 5-10. Initially, it is noted that in rejecting claim 26, the Office Action refers to "TDM" of Kosuge, but Kosuge does not use the term "TDM". Moreover, the Office Action misunderstands the claimed invention. The data exchange units are used for data **received** by the input ports, **not** data **transmitted** by the input ports, and data **transmitted** by the output ports, **not** data **received** by the output ports. Hence, the internal protocol used by the switch of Kosuge **after** the data is **received** by the input ports and **before** the data is **transmitted** by the output ports is inapposite to the protocol used by the switch of Kosuge to receive and transmit data. Further, Kosuge **fails** to mention or even refer to the concept of "exchange units" or "data exchange units" and **fails** to mention how data is received by and transmitted from the terminals on the left and right sides of Figure 1. Kosuge, column 3, lines 56-60. Hence, claim 26 is allowable.

Claim 30 recites that: the data are received by the input ports and transmitted by the output ports as **data exchange units**; the data exchange units for packet data comprise **routing information**; the switching of a data exchange unit from a respective input port to a respective output port is controlled by a stored switch configuration; and the stored switch configuration **uses the routing information** of data exchange units for packet data **to determine respective**

output ports to switch the data exchange units. Kosuge fails to teach claim 30 for at least three reasons.

First, Kosuge fails to teach that data are received by the input ports and transmitted by the output ports as **data exchange units**. In rejecting claim 30, the Office Action aligns the recited data exchange units as exchange units to transmit data **from** input **to** output port. The Office Action fails to point to any citation in Kosuge in rejecting claim 30. Based on the same analysis presented above for claim 26, claim 30 is allowable for a first reason.

Second, Kosuge fails to teach that the data exchange units for packet data comprise **routing information**. In rejecting claim 30, the Office Action aligns the recited the data exchange units for packet data with no specific component of the switch 10 in Figure 1 and only points with generality to the switch 10 in Figure 1. The Office Action also fails to point to any citation in Kosuge in rejecting claim 30. As discussed above for claim 26, the Office Action **misunderstands** what a data exchange unit is. Further, Kosuge **fails** to teach how packet switching data is received by and transmitted from the terminals on the left and right sides in Figure 1, and what this data comprises, namely routing information. Kosuge, column 3, lines 56-60. Hence, claim 30 is allowable for a second reason.

Third, Kosuge fails to teach that the stored switch configuration **uses the routing information** of data exchange units for packet data **to determine respective output ports** to switch the data exchange units. In rejecting claim 30, the Office Action aligns the recited stored switch configuration with the control section 14 in Figure 1 to control and route information through the switch 10. The Office Action also fails to point to any citation in Kosuge in rejecting claim 30. As discussed above for claim 26, the Office Action **misunderstands** what a data exchange unit is. Further, Kosuge **fails** to teach how packet switching data received by the

terminals on the left side of Figure 1 are used to determine the respective terminals to switch the packet switching data. Kosuge, column 3, lines 56-60. Further, Kosuge **fails** to teach that routing information is from the data exchange units and **fails** to teach that routing information from data exchange units is used to switch packet data. Hence, claim 30 is allowable for a third reason.

Claims 31-34

Claim 31 recites a method for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising: switching a TDM data from an input port to an output port, which comprises storing the TDM data in a single shared memory based on a time slot of a frame in which the TDM data was received; and switching a packet data from an input port to an output port, which comprises storing the packet data in said shared memory.

For at least two reasons, Kosuge fails to teach claim 31. First, Kosuge fails to teach storing the TDM data in a single shared memory based on a time slot of a frame in which the TDM data was received. Based on the same analysis presented above for the first reason regarding claim 13, claim 31 is allowable for a first reason.

Second, Kosuge fails to teach a single shared memory. Based on the same analysis presented above for the third reason regarding claim 13, claim 31 is allowable for a third reason.

Claims 32-33 are dependent from claim 31 and are allowable as being dependent from an allowable claim.

Further, claim 32 recites that the TDM data is stored in a preselected area of the single shared memory, and that the **preselected area** is based on **a time slot in a frame** in which the TDM data was received by the input port. In rejecting claim 32, the Office Action does not

specifically address the limitations of claim 32 but, instead, pools the rejection of claim 32 with the rejection of claim 31. As discussed above in the analysis for the first reason of claim 13, Kosuge teaches in Figure 13 storing data R0 to R4 for circuit switching calls in blocks 0 and 1 of memory 11 based on **"do not block replacement prevention" flags 21** and **"block replacement order" flags 22**. Kosuge, column 11, lines 49-67; column 12, lines 10-11. The "do not block replacement prevention" flags 21 and "block replacement order" flags 22 are **unrelated** to a time slot of a frame in which the data for a circuit switching call was received. Hence, claim 32 is allowable.

Claim 33 recites that the **output port** for the **TDM data** is determined based on **the time slot in the frame** in which the TDM data was received by the input port, and that the **output port** for the **packet data** is determined based on **routing data embedded** in the packet data and based on the **input port** which received the packet data. In rejecting claim 33, the Office Action does not specifically address the limitations of claim 33 but, instead, pools the rejection of claim 33 with the rejection of claim 31. Although Kosuge discusses how data moves through the switch 10, Kosuge is silent as to how the respective output ports for circuit switching data and packet switching data are actually determined. See, e.g., Kosuge, Figure 5; column 6, lines 1-32. Hence, claim 33 is allowable.

Claim 34 recites limitations similar to those recited for claim 31 and is allowable for reasons similar to those discussed above for claim 31.

Claims 35-40

Claim 35 recites a switch for switching TDM data and packet data from input ports to output ports, comprising: a plurality of input ports to receive data, wherein each data comprises

either TDM data or packet data; a plurality of output ports to transmit switched data; a shared memory coupling the input ports to the output ports; a time slot interchange controller coupled to the shared memory to select addresses in the shared memory to store TDM data; and a packet switch controller coupled to the shared memory to select addresses in the shared memory to store packet data. The shared memory is adapted to receive sequentially the data received from the input ports and to switch a sequentially received data from a respective input port to a respective output port. The time slot interchange controller is adapted to select an address of the shared memory for a TDM data based on a time slot of a frame in which the switch received the TDM data. The packet switch controller is adapted to select an address of shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data.

For at least three reasons, Kosuge fails to teach claim 35. First, Kosuge fails to teach a time slot interchange controller to select an address of the shared memory for a TDM data based on a time slot of a frame in which the switch received the TDM data. Based on the same analysis presented above for the first reason regarding claim 13, claim 35 is allowable for a first reason.

Second, Kosuge fails to teach a packet switch controller to select an address of shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data. Based on the same analysis presented above for the second reason regarding claim 13, claim 35 is allowable for a second reason.

Third, Kosuge fails to inherently teach a time slot interchange controller. Based on the same analysis presented above for the fourth reason regarding claim 21, claim 35 is allowable for a third reason.

Claims 36-40 are dependent from claim 35 and are allowable as being dependent from an allowable claim.

Further, claim 38 recites that the shared memory treats the input ports as logical input ports. Based on the same analysis presented above regarding claim 24, claim 38 is allowable for a third reason.

Claim 39 recites that the shared memory places sequentially received packet data in a queue for a respective output port. Based on the same analysis presented above regarding claim 25, claim 39 is allowable.

Claim 40 recites that the data are received by the input ports and transmitted by the output ports as data exchange units. Based on the same analysis presented above regarding claim 26, claim 40 is allowable.

Claims 41-49

Claim 41 recites a switch to switch time division multiplexed (TDM) data and packet data from input ports to output ports, comprising: a plurality of input ports to receive TDM data and packet data, each TDM data having an associated time slot of a frame; a plurality of output ports to transmit switched data; and a single shared memory to switch TDM data and packet data from the input ports to the output ports. The single shared memory is adapted to store TDM data received at the input ports based on the time slot of the frame of each TDM data, and to store packet data received at the input ports based on routing data embedded in each packet data and based on which input port received each packet data.

For at least three reasons, Kosuge fails to teach claim 41. First, Kosuge fails to teach a single shared memory to store TDM data received at the input ports based on the time slot of the

frame of each TDM data. Based on the same analysis presented above for the first reason regarding claim 13, claim 41 is allowable for a first reason.

Second, Kosuge fails to teach a single shared memory to store packet data received at the input ports based on routing data embedded in each packet data and based on which input port received each packet data. Based on the same analysis presented above for the second reason regarding claim 13, claim 41 is allowable for a second reason.

Third, Kosuge fails to teach a single shared memory. Based on the same analysis presented above for the third reason regarding claim 13, claim 41 is allowable for a third reason.

Claims 42-49 are dependent from claim 41 and are allowable as being dependent from an allowable claim.

Further, claim 43 recites that single shared memory is adapted to treat the input ports as logical input ports. Based on the same analysis presented above regarding claim 24, claim 43 is allowable.

Claim 44 that single shared memory is adapted to place sequentially received packet data in a queue for a respective output port. Based on the same analysis presented above regarding claim 25, claim 44 is allowable.

Claim 45 recites that the input ports are adapted to receive and the output ports are adapted to transmit TDM data and packet data as data exchange units. Based on the same analysis presented above regarding claim 26, claim 45 is allowable.

Claim 46 recites the data exchange units for packet data comprise routing information used to determine output ports to switch the data exchange units. Based on the same analysis presented above regarding claim 30, claim 46 is allowable.

Claim 48 recites, *inter alia*, a **time slot interchange controller** external to and coupled to the single shared memory to direct the single shared memory regarding storage of TDM data. In rejecting claim 48, the Office Action does not specifically address the limitations of claim 48 but, instead, pools the rejection of claim 48 with the rejection of claim 41. As discussed above in the analysis for the fourth reason of claim 21, the Office Action asserts that Kosuge inherently teaches a time slot interchange controller. Based on the same analysis presented above for the fourth reason regarding claim 21, claim 48 is allowable.

Claims 50-53

Claim 50 recites a method to switch time division multiplexed (TDM) data and packet data, comprising: receiving TDM data and packet data at a plurality of input ports; storing received TDM data in a single shared memory based on a time slot of a frame of each TDM data; storing received packet data in the single shared memory based on routing data embedded in each packet data and based on which input port received each packet data; and forwarding stored TDM data and packet data from the single shared memory to the output ports.

For at least three reasons, Kosuge fails to teach claim 50. First, Kosuge fails to teach storing received TDM data in a single shared memory based on a time slot of a frame of each TDM data. Based on the same analysis presented above for the first reason regarding claim 13, claim 50 is allowable for a first reason.

Second, Kosuge fails to teach storing received packet data in the single shared memory based on routing data embedded in each packet data and based on which input port received each packet data. Based on the same analysis presented above for the second reason regarding claim 13, claim 50 is allowable for a second reason.

Third, Kosuge fails to teach a single shared memory. Based on the same analysis presented above for the third reason regarding claim 13, claim 50 is allowable for a third reason.

Claims 51-53 are dependent from claim 50 and are allowable as being dependent from an allowable claim.

Further, claim 51 recites that TDM data are stored in a preselected area of the single shared memory based on the time slots of the frames. Based on the same analysis presented above regarding claim 32, claim 51 is allowable.

Claim 53 recites that the output ports for TDM data are determined based on the time slots of the frames, and that the output ports for packet data are determined based on the embedded routing data and based the input ports which received the packet data. Based on the same analysis presented above regarding claim 33, claim 53 is allowable.

3. Claims 13, 31-35, and 53 are amended to correct typographical errors and clarify the invention, but not to overcome any claim objections or rejections.

4. Claims 54-62 are added. Claim 54 depends from claim 21, claims 55 and 56 from claim 32, claim 57 from claim 35, claim 58 from claim 37, claims 59 and 60 from claim 42, claim 61 from claim 48, and claim 62 from claim 51. As claims 21, 32, 35, 37, 42, 48, and 51 are allowable as discussed above, claims 54-62 are likewise allowable.

5. The fee of $162 is being submitted herewith for nine further additional claims in excess of twenty (9 X $18 = $162). If no check is attached, or if a greater or lesser fee is

required, please charge or credit Deposit Account Number 22-0261 accordingly and notify the undersigned.

THEREFORE, because all objections and rejections have been overcome, it is submitted that claims 13, 21-26, and 28-62 are allowable, and such allowance is requested.

Respectfully submitted,

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